REMARKS

Claims 1-23 are pending in this application and are subject to examination. In the Office Action mailed March 15, 2006, claims 5-7, 8-10, 15-17, and 18-20 were rejected under 35 U.S.C. §112; claims 1-5, 11-15, and 21-23 were rejected under 35 U.S.C. §102, and claims 6, 8, 9, 16, and 18-19 were rejected under 35 U.S.C. §103. By this Amendment, claims 1, 5, 7-8, 10-11, 15, 17-18, and 20-21 have been amended.

Claim Rejections-35 U.S.C. §112

Claims 5-7, 8-10, 15-17, and 18-20 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. By this Amendment, claims 5, 7-8, 10, 15, 17-18, and 20 have been amended to overcome this rejection. In light of the amendments to the claims, withdrawal of the rejection is respectfully requested.

Claim Rejections-35 U.S.C. §102

Claims 1-5, 11-15, and 21-23 stand rejected under 35 U.S.C. §102(a), as being anticipated by JP-2003-202362 to Masatake ("Masatake"). It is noted that claims 1, 5, 7-8, 10-11, 15, 17-18, and 20-21 have been amended by this Response. To the extent that the rejection remains applicable to the claims currently pending, the rejection is hereby traversed, as follows.

Amended claim 1 is directed to a method for testing an integrated circuit using dual scan chains. The method includes scanning a first test data from an input pin into a first scan chain during a first state of a clock cycle and scanning a second test data from the input pin into a second scan

chain during a second state of the clock cycle. The clock cycle is directly input to the first scan chain and the second scan chain during testing.

Masatake teaches a scan test circuit with a shift register 11 and a shift register 12 which constitute two scan chains. A scan clock CLK is provided to the first scan chain 11. See Masatake, Abstract and Figure 1. As described in page 6 of Masatake, "The inverter 2 reverses the scanning clock CLK and outputs the reversal clock BCK. The selector 3...answers supply of the scanning enable signal EN, chooses either of the scanning clock CLK and the reversal clock BCK... and is supplied to the scanning clock pin of a shift register 12....[T]he selector 3 for...shift register 12 outputs the scanning clock CLK, when the scanning enable signal EN is "L", and the reversal clock BCK is outputted...at the time of "H." See Masatake, paragraphs [0038] – [0039]

In Masatake, the scan clock CLK is provided to the first shift register 11. When the scanning enable signal EN is low, the reversal (i.e., inverted) clock signal BCK is provided to the second shift register 12. When the scanning enable signal EN is high, the scan clock CLK is provided to the second shift register 12. As the scanning enable signal EN is high during testing and low during normal operation of the circuit, the function of the inverter 2 and the selector 3 is to provide a reversed, or inverted, clock signal to the second shift register 12 during testing, and to provide the scan clock signal CLK to the second shift register 12 during normal operation. Thus, Masatake does not teach or suggest the limitation of "the clock cycle is directly input to the first scan chain and the second scan chain during testing," as recited in amended claim 1. For this reason, claim 1 is patentable over the art of record.

Claims 11 and 21 recite similar language to amended claim 1 and are patentable for similar reasons to those cited above with reference to claim 1. Dependent claims 2-10, 12-20, and 22-23 are

dependent on independents claim 1, 11, and 21, respectively, and define further features of the invention. Dependent claims 2-10, 12-20, and 22-23 are patentable for at least those reasons discussed above with reference to the independent claims.

CONCLUSION

Based on the foregoing, all claims are now allowable and a Notice of Allowance is respectfully requested. If the Examiner has any questions or comments regarding this amendment, the Examiner is respectfully requested to contact the undersigned at (650) 849-4400. The Commissioner is authorized to credit any overpayment or to charge any underpayment to Bingham McCutchen's Deposit Account No. **50-2518,** referencing billing number **7035962001**.

Respectfully submitted,
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